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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/433,389 | 11/03/1999 | KOJI OGUMA | 51441-016 | 2492 |

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| EXAMINER | |
|---|---|
| NELSON, ALECIA DIANE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2675 | 20 |

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/433,389 | OGUMA, KOJI | |
| | Examiner | Art Unit | |
| | Alecia D. Nelson | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 2-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 2, 3, 6, and 7*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endoh et al. (U.S. Patent no. 5,218,352) in view of Chihara (U.S. Patent No. 4,196,432).

With reference to **claims 2, 3, 6, and 7**, Endoh et al. teaches a passive matrix liquid crystal display circuit comprising a bias producing means (3) for producing 1/3 bias. The power switching means (8) supplies a voltage (VDD), which is divided by resistors (R1, R2, R3, and R') to provide output voltages (VLC0, VLC1, VLC2). These output voltages are used as bias voltages for display driving means (2). Endoh et al. fails to specifically teach the layout of the LCD display as claimed, however it is a structure, which is well known to those skilled in the art.

Even though Endoh et al. teaches that there is a bias changing means (9), which is connected with bias producing means (3), serving to change the resistance of a resistor (R') for producing the bias voltage (VLC2), wherein that the changing means (9) changes the bias voltage (VLC2) in accordance with the power supply changing command signal (A) thereby to reduce the contrast to some degree in order to prevent

the contrast from becoming to high (see column 7, lines 30-40), and by increasing the resistance of resistor (R'), the LCD driving voltage becomes smaller (see column 7, lines 52-56) and as seen in Fig. 4, a dormant period for which the voltage between all common and segment terminals is close to zero in a single frame period, there is no disclosure of the usage of a the controller including a dormancy determining means for selecting within a single frame at least one predetermined period for which the voltage between all common and segment terminals is zero.

Chihara teaches a LCD composed of a divider circuit (2) comprises of a plurality of divider stages, which divide down the high frequency signals and apply a low frequency signal (see column 3, lines 55-67), wherein the liquid crystals are rendered visually distinguishable when the segment electrodes are energized to a potential opposite the potential of the common electrode, to thereby effect a sufficient potential difference there between. A signal (S9) represents the potential difference defined between the common electrode and segment electrode produced as a result of the common output signal and segment output signal being applied to the display cell, wherein during a period (tc) there is no potential difference between the common electrode and segment electrode of the display cell and thereby permit same to be substantially transparent and not perceived by the human eye (see column 6, lines 11-45).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the circuitry of Chihara to be included in the bias producing means of Endoh et al. in order to allow the potential difference between the common

and segment electrodes to be zero to thereby provide improved density adjustment preventing the user from receiving an unusual impression of the display by suppressing a change in the contrast thereof while reducing power consumption.

3. ***Claims 4 and 5*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endoh et al. in view of Chihara as applied to claim 3 above, and further in view of Yammamoto (U.S. Patent No. 5,515,074).

With reference to **claims 4 and 5**, Endoh et al. and Chihara fail to specifically teach that the controller includes a dormancy discarding means responsive to the signals from the input means for making a decision as to whether or not the dormant period is put in the frame period.

Yammamoto teaches the usage of a data I/O device (15), which performs input/output of density data to/from the main memory (14) (see column 3, lines 4-20), a temperature sensor (16), which detect an environmental temperature of the display device, and a manual control volume (17), which performs manual control of the density and is connected to the control circuit (11) wherein the control circuit 911) further includes an automatic temperature follow-up controller for automatically performing fine adjustment of the density with a change in environmental temperature of the display device during its use (see column 3, lines 24-30). Further it is taught when the detected temperature is compared with the stored data in the memory and the data can not be

applied the density is calculated corresponding to the detected temperature data and the display is adjusted according to the new data (See Figure 2).

Therefore it would have been obvious to use the temperature detection means, and the manual control to generate display data according to detected environmental temperature, as taught by Yammamoto, along with the electronic device similar to that which is taught by Endoh et al. and Chihara wherein the voltage applied between the segment and common electrodes are driven in a manner to render the liquid crystal display cell substantially transparent in order to not be perceived by the human eye in order to thereby provide an automatic or manual adjustment so that the environmental temperature of the display device changes with a change in operation environment of the display device for providing optimum display characteristics to the user.

***Response to Arguments***

4. Applicant's arguments filed 5/26/04 have been fully considered but they are not persuasive. It is argued by the applicant that while Endoh teaches a passive matrix type liquid crystal display device, Chihara teaches the usage of an active matrix type display device, however there is no citation given for these teachings. The examiner finds no disclosure in Chihara directed towards the device being of active matrix type. There is taught a first drive circuit coupled to a common electrode of each display cell for alternately referencing the common electrode between first and second opposite potentials for a predetermined interval of time, and a second drive circuit coupled to the segment electrode defining each display cell for selectively referencing the segment

electrode to a potential opposite in polarity of the potential of the common electrode to define a predetermined potential difference between the common electrode and segment electrode (see abstract). Further it is argued that the combination of the reference does not teach the resulting difference between all of the common and segment terminal is zero during a period within a single frame. However, Endoh teaches a dormant period for which the voltage between all common and segment terminals is close to zero in a single frame period. Chihara teaches represents the potential difference defined between the common electrode and segment electrode produced as a result of the common output signal and segment output signal being applied to the display cell, wherein during a period (tc) there is no potential difference between the common electrode and segment electrode of the display cell. Therefore the claimed limitations are taught by the combination of the reference. With reference to Yamamoto, the applicant argues the usage of the D/A converter (12) is an analog circuit and would be costly if it were included on the same chip as an associated control circuit that is a digital circuit. However, as stated in the rejection Yamamoto is used in combination to teach the controller includes a dormancy discarding means responsive to the signals from the input means for making a decision as to whether or not the dormant period is put in the frame period. Therefore the teachings of Yamamoto teach the usage of the claimed circuitry in a controller. Therefore it would be obvious for the controller of Endoh to include the circuitry for making the determinations as claimed.

The rejection to the claims will be maintained and the rejection will be made final.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
October 16, 2004

Amr Ahmed Awad

AMR A. AWAD
PRIMARY EXAMINER